

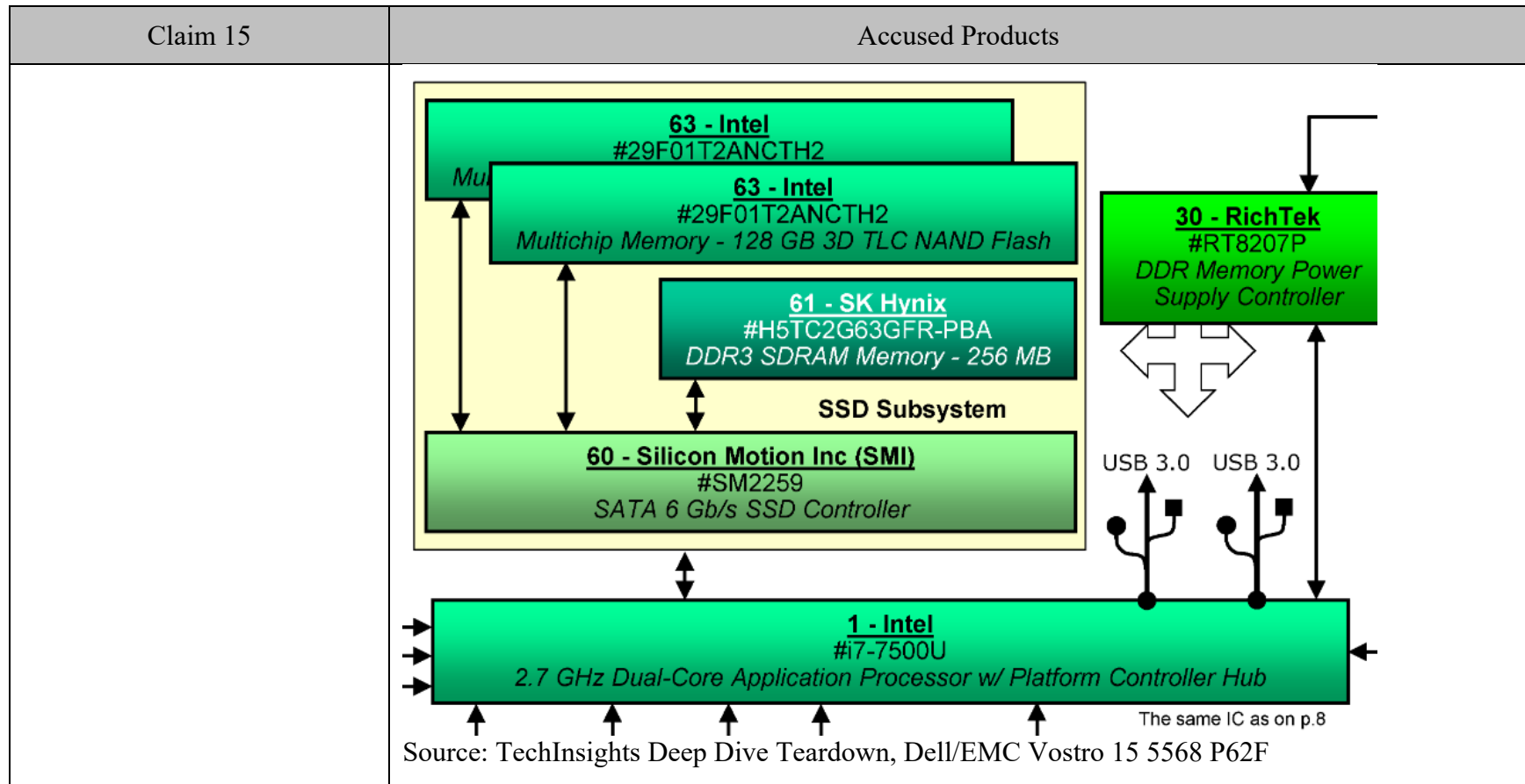
Exhibit 4

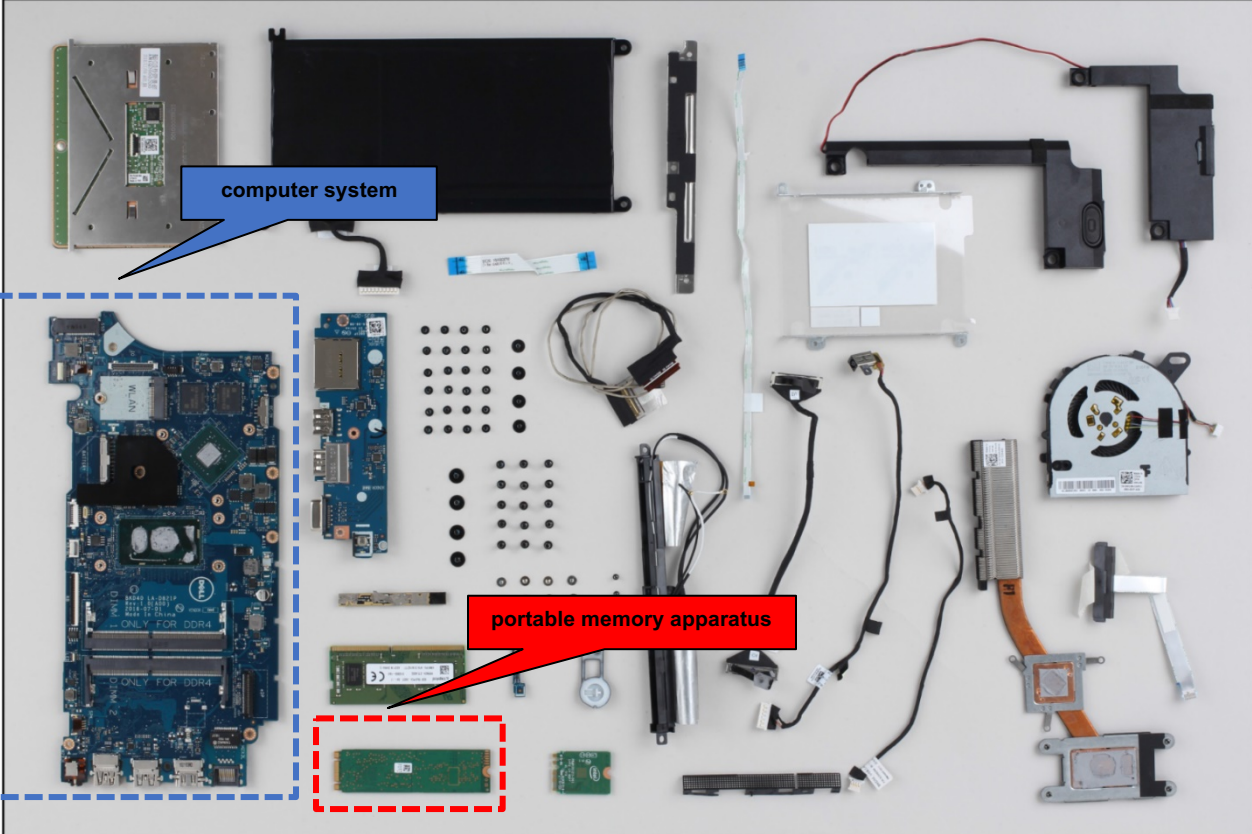
U.S. Patent No. 6,920,527 (“’527 Patent”)**Accused Products**

Dell/EMC products with SSDs including Silicon Motion SSD Controllers, including without limitation the Dell/EMC Vostro 15 5568 P62F (“Accused Products”), infringe at least Claim 15 of the ’527 Patent.

Claim 15

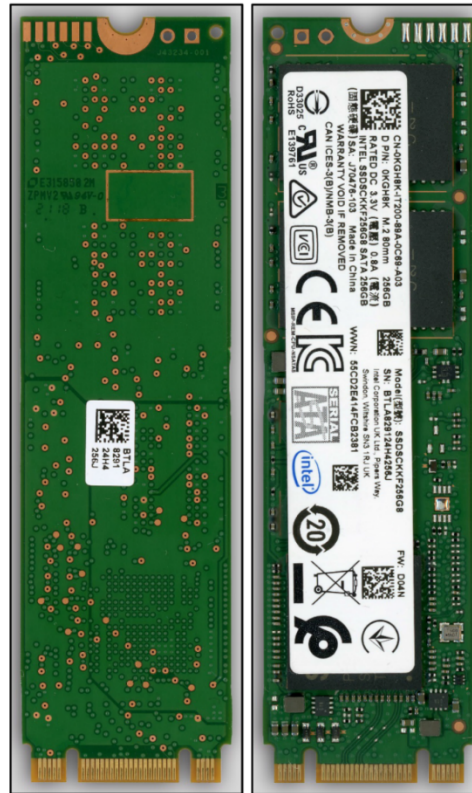
Claim 15	Accused Products
[15pre]. A method, comprising:	To the extent the preamble is limiting, each Accused Product practices the claimed method. <i>See</i> limitations [15a]-[15d] below.
[15a] coupling a portable memory apparatus to a computer system, wherein said portable memory apparatus comprises a memory controller chip, a non-volatile memory, and a volatile memory;	Each Accused Product performs coupling a portable memory apparatus to a computer system, wherein said portable memory apparatus comprises a memory controller chip, a non-volatile memory, and a volatile memory. For example, the Dell/EMC Vostro 15 5568 P62F couples an Intel SSDSCKKF256GB SSD to a computer system. The SSD in part comprises a Silicon Motion Inc SM2259 memory controller, an Intel 29F01T2ANCTH2 3D TLC NAND Flash array, and an SK Hynix H5TC2G63GFR-PBA DDR3 SDRAM volatile memory array. <i>See, e.g.:</i>



Claim 15	Accused Products
	 <p data-bbox="640 1104 1885 1144">Source: TechInsights Deep Dive Teardown, Dell/EMC Vostro 15 5568 P62F</p>

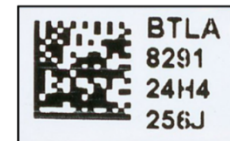
Claim 15

Accused Products

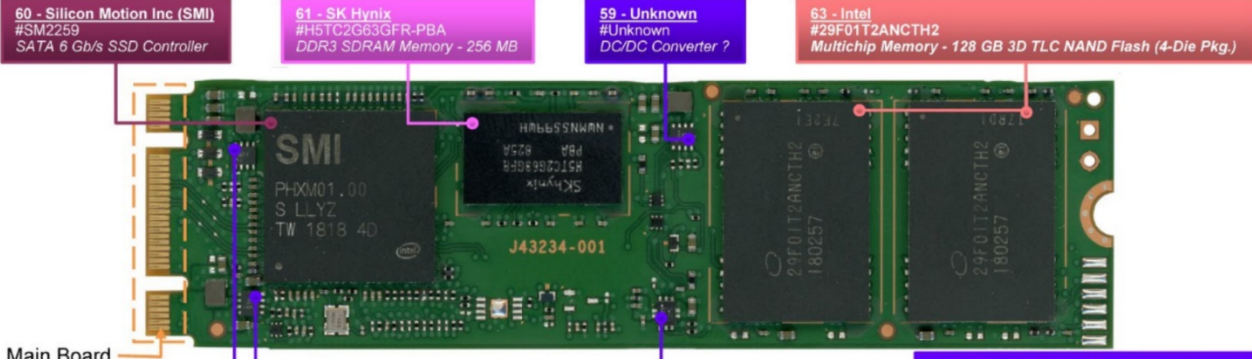
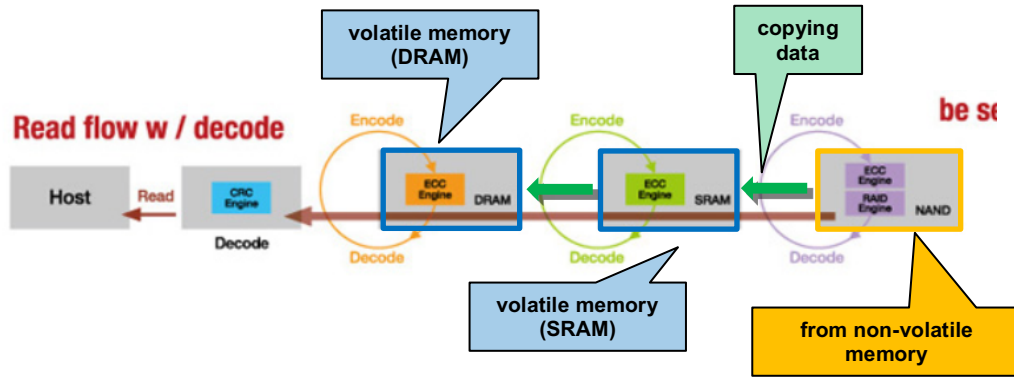


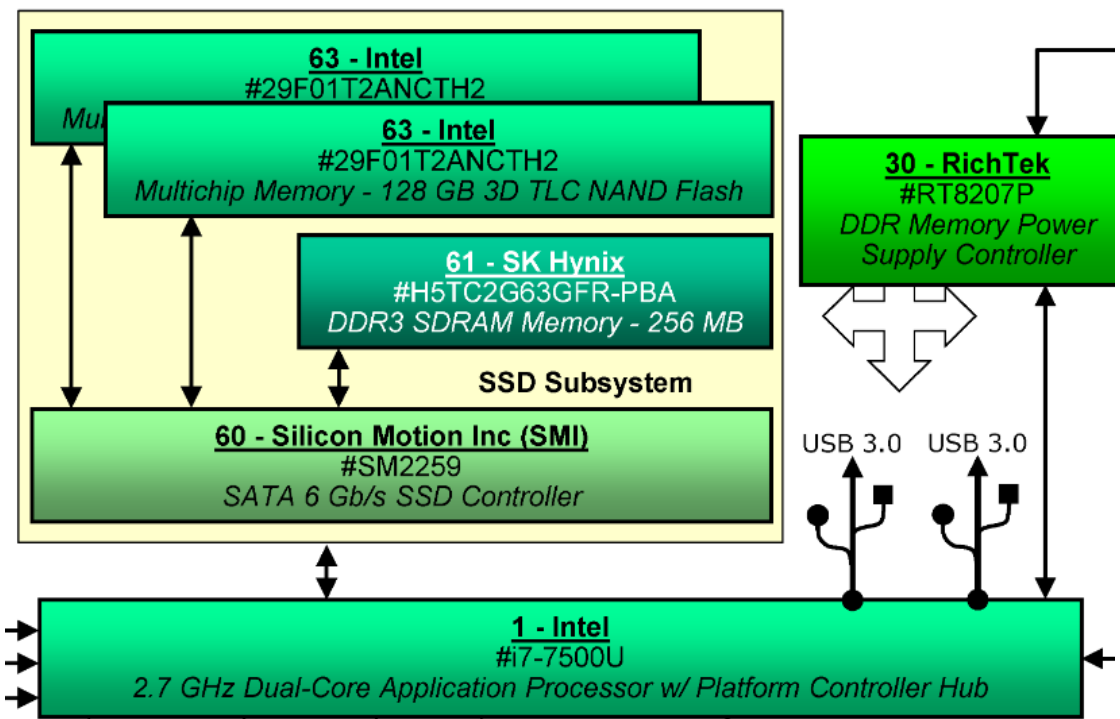
SSD Subsystem		
Brand	Intel	
Part Number	SSDSCCKKF256GB	
Module Dimensions	80 x 22 x 1.95	
Weight (grams)	5.62	
Estimated Costs	Electronic Parts	\$32.72
	Non-Electronic Parts	\$0.07
	Assembly	\$1.07
	Test	\$0.15
	Gross Margin	\$8.50
Estimated Module Price		\$42.51

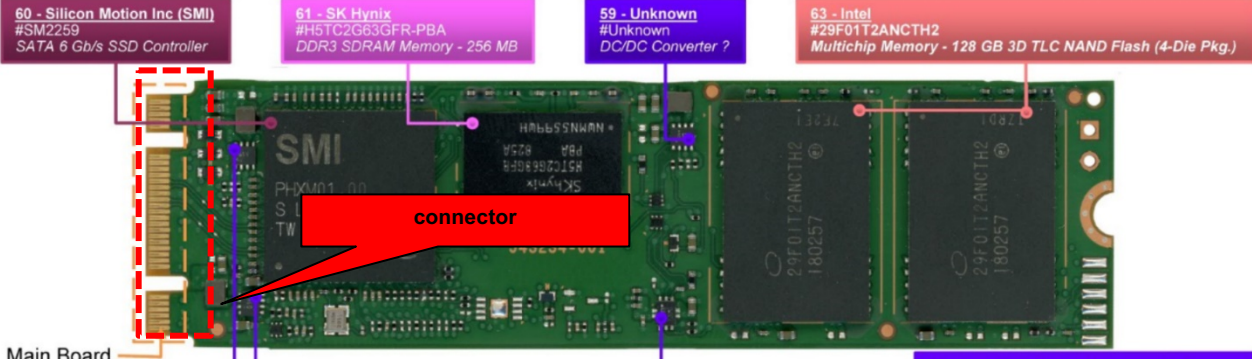
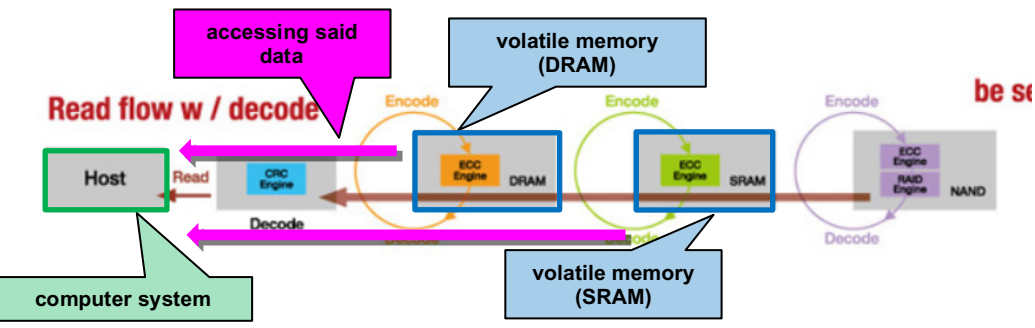
A full Subsystem BOM is provided in the included BOM workbook.

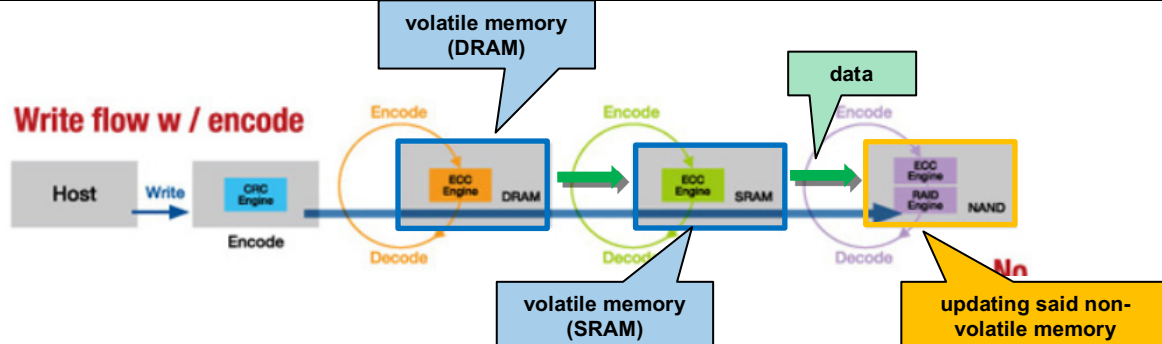


Source: TechInsights Deep Dive Teardown, Dell/EMC Vostro 15 5568 P62F

Claim 15	Accused Products
	 <p>60 - Silicon Motion Inc (SMI) #SM2259 SATA 6 Gb/s SSD Controller</p> <p>61 - SK Hynix #H5TC2G63GFR-PBA DDR3 SDRAM Memory - 256 MB</p> <p>59 - Unknown #Unknown DC/DC Converter ?</p> <p>63 - Intel #29F01T2ANCTH2 Multichip Memory - 128 GB 3D TLC NAND Flash (4-Die Pkg.)</p> <p>Main Board</p> <p>Source: TechInsights Deep Dive Teardown, Dell/EMC Vostro 15 5568 P62F</p>
<p>[15b] copying data from said non-volatile memory to said volatile memory using said memory controller chip;</p>	<p>Each Accused Product performs copying data from said non-volatile memory to said volatile memory using said memory controller chip.</p> <p>For example, during a memory read the SM2259 memory controller copies data from the non-volatile NAND flash memory to the volatile memory (SRAM and DRAM).</p> <p>See, e.g.:</p>  <p>Source: http://www.siliconmotion.com/A3.2_Overview_Detail.php?sn=1</p>

Claim 15	Accused Products
<p>[15c] accessing said data in said volatile memory using said computer system through a connector coupled to said portable memory apparatus and said memory controller chip; and</p>	<p>Each Accused Product performs accessing said data in said volatile memory using said computer system through a connector coupled to said portable memory apparatus and said memory controller chip.</p> <p>For example, the computer system accesses the data by communicating with the SM2259 SSD controller through the M.2 connector coupled to the SSD and SSD controller.</p> <p><i>See, e.g.:</i></p>  <p>Source: TechInsights Deep Dive Teardown, Dell/EMC Vostro 15 5568 P62F</p>

Claim 15	Accused Products
	 <p>Source: TechInsights Deep Dive Teardown, Dell/EMC Vostro 15 5568 P62F</p>  <p>Source: http://www.siliconmotion.com/A3.2_Overview_Detail.php?sn=1</p>
[15d] updating said non-volatile memory with data from said volatile memory.	<p>Each Accused Product performs updating said non-volatile memory with data from said volatile memory.</p> <p>For example, the SM2259 SSD updates the NAND flash array using the contents of the volatile DRAM and SRAM memories.</p> <p><i>See, e.g.:</i></p>

Claim 15	Accused Products
	 <p>The diagram illustrates the 'Write flow w / encode' process. It starts with a 'Host' sending a 'Write' command to a 'CRC Engine' which performs an 'Encode' operation. The data then moves to a block containing an 'ECC Engine' and 'DRAM', labeled as 'volatile memory (DRAM)'. From there, it goes to another block with an 'ECC Engine' and 'SRAM', labeled as 'volatile memory (SRAM)'. Finally, the data is sent to a block with an 'ECC Engine', 'RAID Engine', and 'NAND', labeled as 'updating said non-volatile memory'. The flow is marked with 'Encode' and 'Decode' steps at each transition. A 'data' box is also shown. A red 'No' is written next to the final NAND block.</p> <p>Source: http://www.siliconmotion.com/A3.2_Overview_Detail.php?sn=1</p>